United States Patent

[11] 3,629,939

[72] Inventor **Ralph H. Baer**
Manchester, N.H.

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[45] Patented **Dec. 28, 1971**

[73] Assignee **Sanders Associates, Inc.**
Nashua, N.H.

Original application Feb. 10, 1965, Ser. No. 431,558, now abandoned. Divided and this application Feb. 10, 1969, Ser. No. 811,268

[54] **MULTILAYER CORE MEMORY PROCESS**
8 Claims, 18 Drawing Figs.

[52] **U.S. Cl.** ..... **29/604 R,** 29/627 R, 156/3 R, 204/15 R, 117/212 R, 264/272 R, 340/174 MA
[51] **Int. Cl.** **H01f 7/06**
[50] **Field of Search** ..... 29/604, 625, 627, 626; 340/174 MA; 117/212; 156/3; 264/272; 204/15

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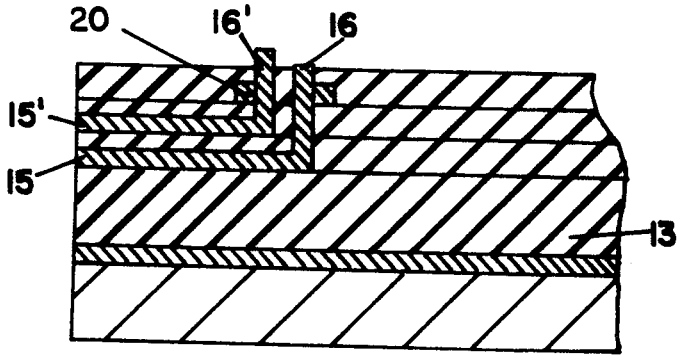
Primary Examiner—John F. Campbell
Assistant Examiner—Robert W. Church
Attorney—Louis Etlinger

ABSTRACT: A method of making a magnetic core matrix by selectively etching a conductive layer to form horizontal conductors leaving vertically extending conductors over which apertured cores are disposed. The vertical conductors are then connected by deposited conductor material thereby threading said core apertures. Insulating material is deposited where needed to secure the cores in place and/or insulate conductive areas.



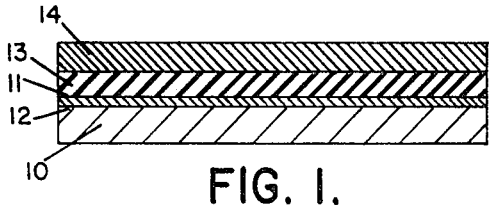


FIG. 1.

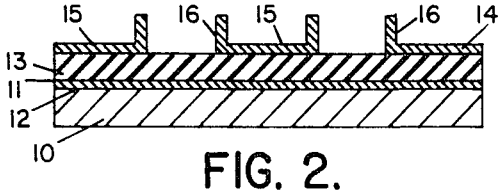


FIG. 2.

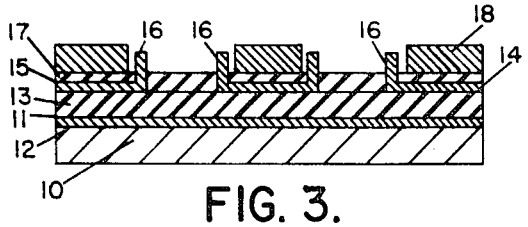


FIG. 3.

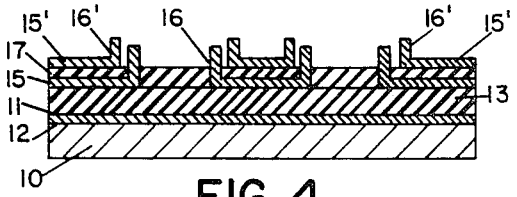


FIG. 4

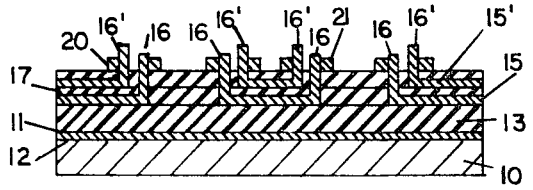


FIG. 5

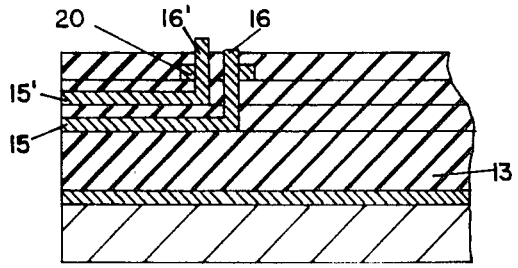


FIG. 5a

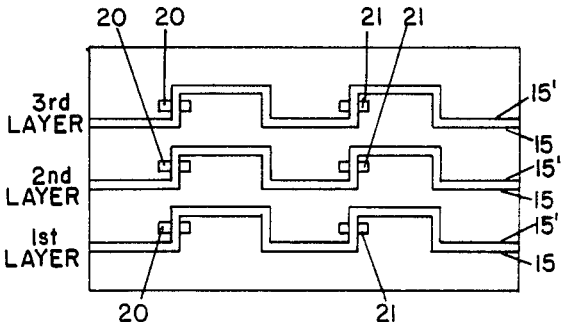


FIG. 6.

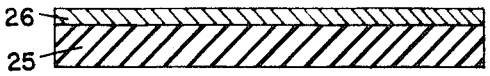


FIG. 7.

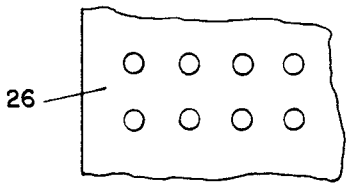


FIG. 8.

INVENTOR

RALPH H. BAER

BY

ATTORNEY

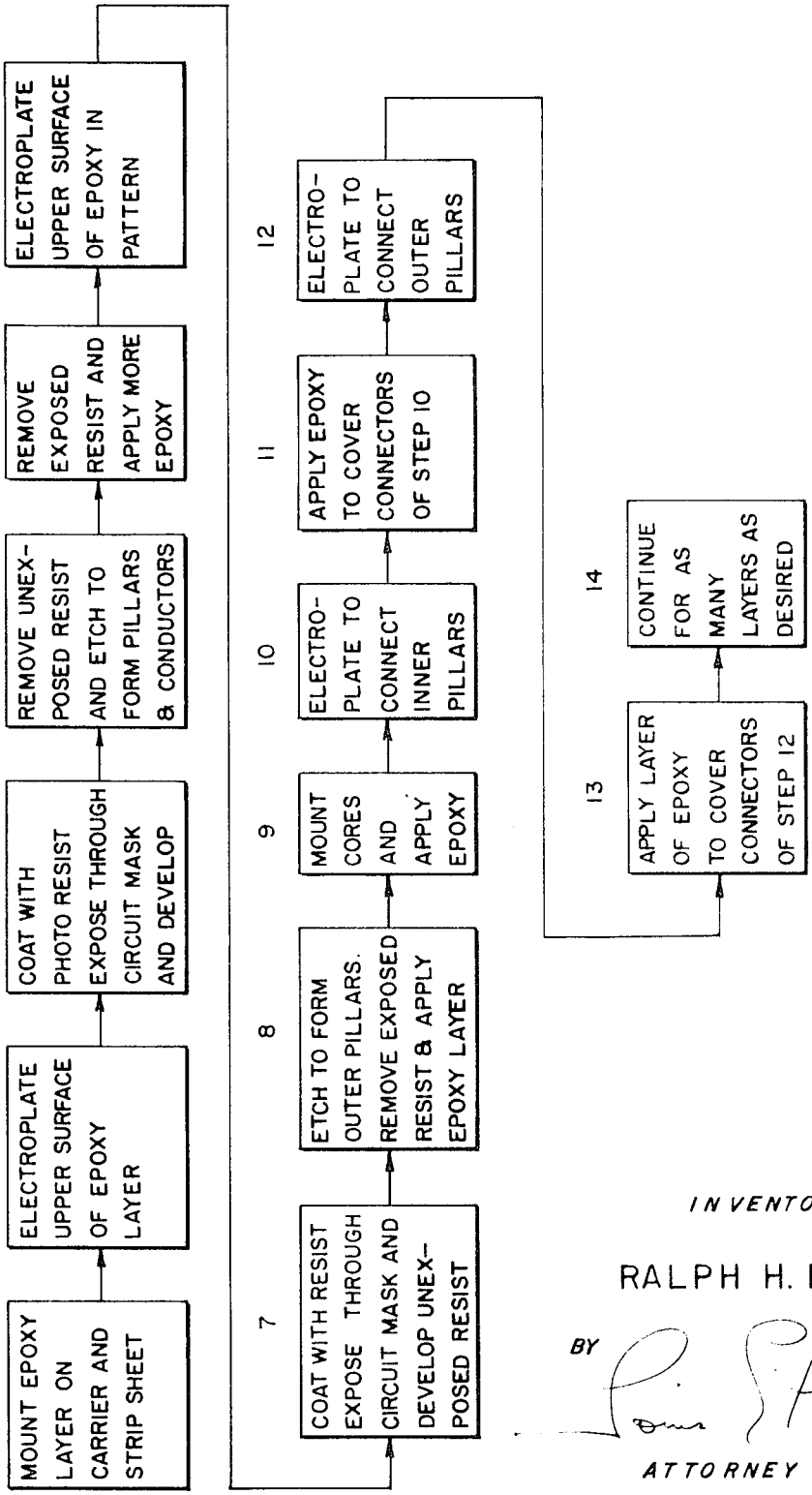


FIG. 9.

INVENTOR

RALPH H. BAER

BY

ATTORNEY

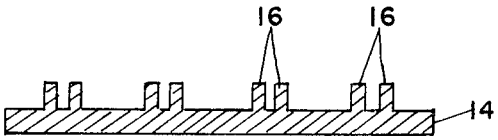


FIG. 10.

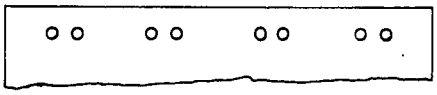


FIG. 11.

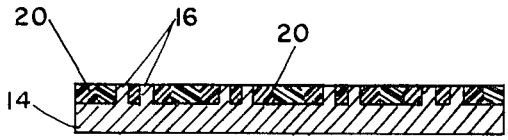


FIG. 12.

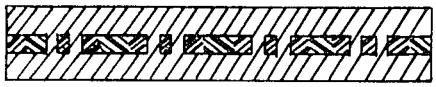


FIG. 13.

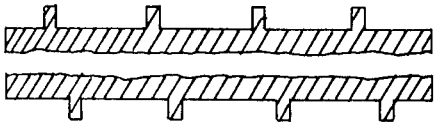


FIG. 14.

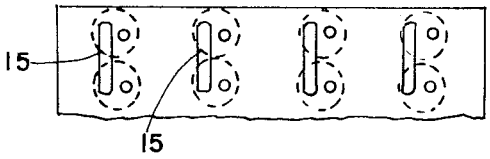


FIG. 15.

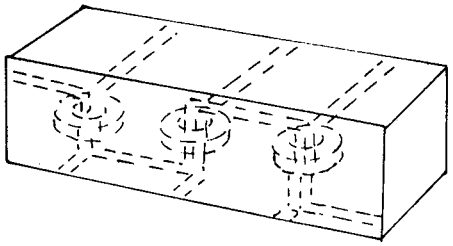


FIG. 16.

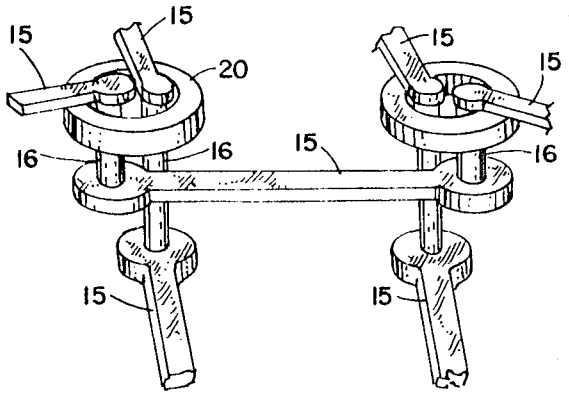


FIG. 17.

INVENTOR

RALPH H. BAER

BY Louis T. Hagopian

ATTORNEY

MULTILAYER CORE MEMORY PROCESS

The present application is a division of my presently pending application Ser. No. 431,558, filed Feb. 10, 1965, and entitled "Multilayer Core Memory" and now abandoned.

Heretofore, such memory boards have been made by wiring, sewing, stitching, or lacing wires by hand or machine through the cores employed, and securing said wiring by soldering. This has proved to be unduly expensive, requiring the use of fine wire and many soldered joints. Additionally, the reliability of boards so made is not as good as desired, and the possibility of error in wiring is high, still further increasing the cost, by requiring extensive testing and the rejection of an unduly high percentage of boards found to be erroneously wired.

By applying the principles hereinafter disclosed, I am able to reduce the cost of core memory boards, eliminate the use of fine wire and soldered joints, greatly increase the reliability of memory circuit boards, and eliminate the possibility of error due to incorrect connections. I am able to utilize techniques proved in the manufacture of printed circuits, as more particularly disclosed and claimed in the copending patent applications of Gerald Boucher, entitled "Printed Circuits and Methods for Producing Same," Ser. No. 277,646, filed May 2, 1963, now U.S. Pat. No. 3,374,129, and "Multilayer Printed Circuit Having Integral Connecting Pins, Sockets or Terminals," Ser. No. 415,378, filed Dec. 2, 1964, and now abandoned, respectively, assigned to the assignee hereof, and to which reference may be had. The disclosure of said applications is to be considered as a part hereof with the same force and effect as if herein set out in writing. By so doing, I am able to establish the manufacture of memory boards on a practical bulk-fabricated basis, rather than the essentially individual manual assembly heretofore employed.

From the foregoing, it will be understood that among the objects of this invention are:

To provide a memory board, and a process for making it, which avoids or eliminates the drawbacks and difficulties heretofore encountered in such boards and the processes for fabricating them,

To provide such a board and a process for making it which eliminates the use of fine wire and soldered joints heretofore employed,

To provide a process for making such boards which eliminates or greatly reduces the possibility of errors in the circuitry employed,

To provide such a board and a process of making it which greatly increases the reliability of the board,

To provide such a board and process for making it in which the cost is substantially reduced,

To provide such a board and process of making it, characterized by uniformity,

To provide such a board and process for making it which is particularly adapted to the use of quantity production methods, and which eliminates, or greatly reduces, the labor and attention to individual boards heretofore necessary.

Still other objects and advantages of my invention will be apparent from the specification.

The features of novelty which I believe to be characteristic of my invention are set forth with particularity in the appended claims.

My invention itself, however, both as to its fundamental principles and as to its particular embodiments, will best be understood by reference to the specification and accompanying drawings, in which

FIG. 1 is a section through a memory board at the start of my process,

FIG. 2 is a similar view after the first electroplating and etching,

FIG. 3 is a similar view after the second electroplating,

FIG. 4 is a similar view after the second etching,

FIG. 5 is a similar view after the cores are placed in position,

FIG. 5*a* is a fragmentary section showing a method of applying the cores,

FIG. 6 is a view similar to FIGS. 1–5 of a completed multilayer board,

FIG. 7 is a section showing a laminate used in making the nickel cores,

FIG. 8 is a fragmentary top plan view showing the laminate of FIG. 7 after the inside diameter core openings have been etched out,

FIG. 9 is a flow diagram of the process according to my invention,

FIG. 10 is a sectional view of a modified form of board according to this invention, after the first etching,

FIG. 11 is a fragmentary top view thereof,

FIG. 12 is a sectional view of the same after the cores are mounted and spaces filled with epoxy or similar material,

FIG. 13 is a similar view after the electroplating of more copper on top of the board,

FIG. 14 is a similar view, partly broken away, after the next etching,

FIG. 15 is a top fragmentary view after a layer of epoxy has been added, and another layer of copper has been added and etched,

FIG. 16 is a perspective view of a completed board, and

FIG. 17 is a perspective view, on an enlarged scale, showing two cores and associated conductors, but omitting, for clarity, the epoxy or similar material.

Referring now more particularly to FIGS. 1 and 2, I may provide a carrier plate 10 of any suitable material, such as glass, metal, or the like, which is preferably covered with a thin sheet 11 of Mylar, Teflon or the like, which may be cemented around the edges as at 12. Above this I preferably provide a sheet 13 of epoxy fiber glass or the equivalent to form the base of the board. The upper surface of the epoxy sheet 13 is next coated with a layer 14 of copper by laminating the epoxy and copper with heat and pressure to the desired thickness, although a stock laminate of the desired thicknesses may be used as the starting material.

At this point, the upper surface of copper layer 14 is covered with a light-sensitive resist, and exposed through a mask having the pattern of conductors 15 and pillars 16 desired. The resist is developed, the unexposed resist removed, and the copper layer etched. All the copper within certain pairs of pillars is removed, either by drilling before etching, or by the further steps of coating with resist, exposing through a mask which exposes all but the resist covering the copper within the pillars which it is desired to remove, dissolving off the resist covering the copper to be removed, and etching again. If the copper between the bases of certain of the pillars were not removed, they would be short circuited by the copper left connecting them, and flux through the cores would not be produced. At the completion of these steps, the board will appear as in FIG. 2.

At this point, another layer 17 of epoxy fiber glass is applied above conductors 15 to cover them, and to fill in partly the opening in pillars 16, and a second layer of copper 18 electroplated over epoxy layer 17, at which point the board will have the appearance shown in FIG. 3. The copper layer 18 is then etched to form a second set of conductors 15′ and pillars 16′, and has the appearance shown in FIG. 4, and is now ready for the application of the cores 20 and 21. These are usually in the form of small toroids or washers, and are placed so as to surround the first, but not the second pillars 16 and 16′ of each group.

After the cores 20 are placed in position, the board will have the appearance shown in FIG. 5.

To complete the board, the top of the board is filled in or coated with epoxy to the level of the top of lower pillars 16, as shown in FIG. 5*a*, which are to be connected in each group. This may be done by electroplating a copper layer over the top of the board, connecting the pillars 16 of each group, while other conductors not to be connected are masked off or protected, then applying another layer of epoxy to the level of pillars 16′ of each group, using the steps already described, and finally applying a final top layer of epoxy to complete the enclosure of the board, except for connectors which may be connected to the various external points desired.

When completed, carrier plate **10** and Mylar or Teflon strip **11** removed, and the board has the appearance, in section, of FIG. **6**, which is also a schematic wiring diagram, with conductors **15** and **15'** threading the cores **20** and **21**, all solidly encased in epoxy **13** except where conductors **15** and **15'** are brought out for external connection.

In order to place the cores in position during fabrication of the board, they may be placed individually at the desired places, as indicated in FIG. **5**. This, however, is a tedious and time-consuming job, and it is preferable to use a carrier or jig to place them all in proper position at one time. If desired, they may all be placed and temporarily cemented on a carrier sheet of uncured epoxy fiber glass, which can then be removed from the jig or fixture and placed, core side down, on top of the layer of epoxy, the spaces filled with epoxy, as in FIG. **5***a*, and the process of fabrication continued as before. On the other hand, uncured epoxy can be utilized as a cover for the cores once secured in place. If necessary, the epoxy carrier can be punched to permit the pillars to pass through it.

The various steps employed in fabricating the board shown in FIGS. **1–6** are indicated in flow diagram, FIG. **9**.

The epoxy fiber glass layer is mounted (step **1**) upon a carrier plate covered by a strip sheet cemented thereto. The upper surface of the epoxy layer is then plated with a metallic conductor, such as copper or silver (step **2**). To facilitate the plating, a first coating of "electroless" copper may be applied, as described in the application above referenced, followed by electroplating to the thickness desired.

The conductive coating is then covered with photoresist (step **3**), exposed through a negative of the circuit desired, including inner pillars and conductors leading to the same, and the board developed. The unexposed resist is removed (step **4**) and the conductor etched, leaving the inner pillars and lowest level of conductors connected to the pillars.

At this point, another layer of epoxy fiber glass is applied over the lowest conductors and bonded to the lowest sheet (step **5**), and another layer of conductor applied to the upper surface to form the outer pillars and conductors leading thereto, using the method already described (step **6**). This coating of conductor thereto is covered with photoresist, exposed through a negative circuit mask of the outer pillars, and conductors leading thereto, developed, and the unexposed resist removed (step **7**).

The conductor is then etched to form the outer pillars and conductors leading thereto, the exposed resist removed, and another layer of epoxy fiber glass applied to the upper surface (step **8**). At this point, both inner and outer pillars project above the surface of the epoxy by a greater distance than the height of the cores.

The board is now ready to receive the cores (step **9**), which may be ferrite, in the form of small beads in this embodiment of the invention, and the cores are placed so that one inner and one outer pillar extend up through the central opening in each ferrite bead, and more epoxy is applied to fill in any empty space and to cover and secure the cores permanently in position. One inner and one outer pillar projecting above the core in each group will then extend above the top epoxy layer.

The board is then electroplated (step **10**) by the process already described, to join the lower conductors **15** in the pattern described, for example, that shown in FIG. **6**, and another layer of epoxy applied to the upper surface to cover conductors **15** (step **11**), leaving only the pillars of conductors **15'** exposed at their upper ends.

Another layer of conductor is deposited, as before, to join the upper ends of the pillars of conductors **15'** (step **12**), and another layer of epoxy is applied to cover the conductors **15'** (step **13**). This completes a single-core layer board. If a multicore layer board is desired, the process may be continued, repeating steps **2–13** each time an additional layer is added. This results in a board such as shown in FIG. **6** in which the cores, with their associated conductors, are three layers deep.

In the foregoing embodiment of the invention, I have shown one embodiment of the invention, in which the cores are non-metallic, such as ferrite. It will be understood, however, that the cores may be of other material, such, for example, as sheet-nickel-type materials having the desired magnetic characteristics. In this case, referring now to FIGS. **7** and **8**, I may produce the cores by starting with a sheet **25** of uncured epoxy fiber glass, to which is laminated a sheet of nickel **26** having the desired magnetic characteristics. The nickel sheet is covered with a layer of photoresist, exposed through a negative mask for the positions of the cores, developed, the unexposed resist dissolved off, leaving the material to form the cores and between the adjacent cores protected by the exposed resist. In one form of the invention, the metal is then etched to remove the nickel from the inside diameter of the cores (at the center) as shown in FIG. **8**. After the center etched nickel sheet which is to form the cores is placed in position and secured, the nickel layer is etched again to form the outside diameter of the cores and remove all extraneous material. In an alternative embodiment, the cores may be etched out completely (both to inside and outside diameters) after they have been mounted on a sheet of B stage (uncured) epoxy material, then the epoxy sheet with the cores is mounted in position with the cores surrounding the selected pillars. This leaves a multiplicity of cores **20** of sheet **25**, and the cores are in the form of small beads, each core having a central opening through which a pair of pillars **16** and **16'** extend, as seen in FIG. **5***a*. The cores and the epoxy carrier are then placed in position as in step **9** of FIG. **9**, and the process is carried on as before with the ferrite-type cores.

Referring now more particularly to FIGS. **10–17**, I have shown a modified form of my invention, as it appears at various stages of the process.

In this modification, I start with a layer of conductor such as copper **14** similar to that shown in FIG. **1** (steps **1** and **2**). This is covered on one side with a layer of photosensitive resist, and exposed through a mask allowing exposure of the resist where the pillars **16** are to be (step **3**). The unexposed resist is then removed (step **4**), and the copper etched to about half its former thickness, leaving the pillars as shown in FIG. **10** and FIG. **11**.

The cores **20** are then placed around each pair of projecting pillars and the upper surface filled in with uncured epoxy or equivalent material to the level of the top of the pillars, and the epoxy cured to lock the cores in place. The upper surface is then ground to the level of the top of the cores, and prepared for electroplating the additional copper, in the manner already described and a layer of copper electroplated onto a thickness substantially equal to that below the cores. At this point a sectional view would appear as in FIG. **13**.

Next, both top and bottom are coated with light-sensitive resist, and exposed through masks allowing exposure where the pillars are to be. Note that in this instance, pillars **16** of each pair are to be on top and bottom of the copper, respectively. After exposure, the unexposed resist is removed and both sides of the copper are etched about halfway through the added copper, leaving the pillars extending on opposite sides, as in FIG. **14**. (In this figure, for simplicity the top and bottom of the board are shown broken away, omitting the cores and the epoxy filling.)

Next, both sides are coated with resist, exposed through a mask protecting the inner layer of printed-circuit conductors, and etched again to leave the inner layer of conductors **15**, joined to pillars **16** as shown in FIG. **15**. In this case it will be noted that I have shown certain of the conductors **15** threading adjacent cores **20** in opposite directions, along one line, and others threading cores in a direction at right angles to the first. Then, both sides of the board are filled with epoxy to the level of the tops of the pillars, the epoxy set, both sides cleaned and electroplated with a final layer of copper. Both sides are then coated with resist, exposed through a mask protecting the outer layers of conductors to be left after etching, and the copper etched away to leave the outer layers of conductors. At this point, both top and bottom are covered with epoxy and cured. This is more clearly shown in FIG. **16**, a per-

spective view of a board of this type, and on an enlarged scale in FIG. 17 which omits the epoxy filling for the sake of clarity. In carrying out the plating, etching, etc. on both sides, this is not intended to mean on both sides simultaneously. First, one side is done, then the other, since many practical difficulties would be encountered in attempting to operate on both top and bottom simultaneously.

In this embodiment, the steps of the process used to form the board as shown in FIGS. 13–17 inclusive, are substantially those described in the referenced applications and as used by the assignee in its "Intramax" process.

In the foregoing I have shown and described my invention, and the best mode presently known to me for practicing the same, but it will be understood that modifications and changes may be made without departing from the spirit and scope of my invention, as will be clear to those skilled in the art.

I claim:

1. The method of forming a core memory board which comprises the steps of providing a layer of conductor upon a layer of insulating material, etching said layer of conductor to form horizontal and vertically extending conducting portions, mounting a plurality of cores each surrounding at least two of said vertically extending portions, applying insulating material to hold said cores in position, electroplating conducting material to complete the pattern of conductors, and applying a coating of insulating material to form a monolithic structure.

2. The method of forming a core memory board which comprises the steps of providing a layer of conductor upon a layer of insulating material, etching said layer of conductor to form horizontal and vertical conducting portions, providing a plurality of cores secured to a sheet of insulating material, mounting said sheet carrying said cores with said cores surrounding parts of said vertical conducting portions, filling in spaces with insulating material, electroplating conducting material to complete the pattern of conductors, and applying a coating of insulating material to form a monolithic structure.

3. The method of forming a core memory board which comprises the steps of etching one side of a conductor plate to leave projecting pairs of pillars, placing one magnetic material core around each of said pairs of pillars, applying insulating material securing said cores in place, depositing a layer of conductor over said insulating material and said pillars, etching both sides of said conductor plate to leave projecting pillars, etching a different pattern to leave an inner layer of conductors joining preselected pillars, applying insulating material over said conductors, depositing conductor over said insulating material, and etching said conductor to leave an outer layer of conductors joining other preselected pillars.

4. The method claimed in claim 3 which includes the step of applying an outer coating of insulating material covering all conductors, leaving only external terminals exposed.

5. The method of forming a magnetic core memory board which comprises the steps of laminating a sheet of magnetic metal to a layer of insulating material, coating said metal with a light-sensitive resist, exposing said resist except in areas to form the openings in said cores, developing said resist, removing the unexposed resist, etching said magnetic metal to form the inner openings in said cores, securing said etched core-forming metal to an insulating board with at least two conductors projecting through each of the openings in said core-forming metal sheet and then etching said magnetic metal again to define the outside diameter of said cores.

6. The method of forming a core memory assembly which comprises the steps of

etching a first layer of conductive material to form a first group of horizontally and vertically extending conductors,

applying to said layer a first coat of insulating material so as to cover said horizontally extending conductors but to leave a portion of said vertically extending conductors exposed,

applying a second layer of conductive material to said coat,

etching said second layer to form a second group of horizontally and vertically extending conductors,

applying a second coat of insulating material so as to cover said horizontally extending conductors of said second group but to leave a portion of all of said vertically extending conductors exposed,

mounting a plurality of magnetic memory cores so that each core encircles at least one vertically extending conductor of each of said first and second groups,

applying a third coat of insulating material so as to cover and retain said cores, and

forming electrical circuitry interconnecting said vertically extending conductors of both groups.

7. The method of forming a core memory assembly according to claim 6 in which said step of forming electrical circuitry includes the steps of

applying a third layer of conductive material over said third coat of insulating material and in electrical contact with all of said vertically extending conductors, and

etching said third layer of conductive material to interconnect said vertically extending conductors in a predetermined circuit configuration.

8. The method of forming a core memory assembly in accordance with claim 7 further comprising the step of

applying a further coat of insulating material over said third layer of conductive material to form a monolithic structure.

* * * * *